REMARKS

Reconsideration and further examination of the subject patent application in light of the present Amendment and Remarks is respectfully requested. Claims 1-9 are currently pending in the application and stand rejected. The claims have been amended to improve the clarity thereof. No new matter has been added.

As a preliminary matter, the undersigned requests that the Office take note of the new attorney docket number of 13322-003, as this docket has been transferred from Welsh & Katz to the undersigned at Brinks Hofer Gilson and Lione.

Remarks Regarding The Drawings

Applicant has submitted replacement sheets to overcome the Examiner's objections. No new matter has been added.

Remarks Regarding The Specification

The specification has been amended to correct typographical errors and other informalities, as required by the Examiner. For purposes of clarity only, a substitute specification is enclosed showing the changes, with new text shown as underlined, and deleted text shown as strikeout. No new matter has been added. Also, a version of the substitute specification incorporating all of the changes ("clean copy of specification") is attached after the signature page. The claims have been omitted from the substitute specification to avoid confusion.

Rejection Under 35 U.S.C. §112

Claims 2-4 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In view of the claims as presently amended, applicant respectfully traverses this rejection. Claim 2 has been amended to recite "a divider." The divider is a common element used

in synchronizing the square wave generator. Claim 4 has been amended to recite "power switch element" rather than "power switch tubes," as suggested by the Examiner. The specification has also been amended for consistency. Other claims have been amended to overcome the objections.

Rejection Under 35 U.S.C. §102

Claims 1, 4, and 6-9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kawabata (US Pat. No. 4,947,310). In view of the claims as presently amended, applicant respectfully traverses this rejection. Applicant submits the Kawabata does not teach or suggest a voltage linear combination circuit in *each* of the plurality of the voltage regulator circuits that linearly combine all of the output voltages of the plurality of voltage regulators, as required by independent claim 1. Kawabata is completely missing this claimed element.

Although Kawabata mentions a voltage regulator for regulating the output voltage of the inverter, such voltage regulation is completely different than applicant's claimed linear combination circuit contained in the voltage regulating unit, as shown in Figures 1 and 8. Kawabata discloses that a node 124 combines the voltage from three sources, namely a voltage control unit 126, capacitor current reference 127, and limiter 125, as shown in Fig. 2 of Kawabata. The combined voltage is provided to a PWM circuit 134 through a limiter 123 and a current control circuit 121.

However, the above-described voltage processing is performed solely within a single inverter device in the Kawabata circuitry. Regulating voltage within a single inverter is a relatively straightforward task. In that regard, applicant's claimed invention includes a voltage linear combination circuit that linearly combine all of the output voltages of the plurality of voltage regulators for all of the inverters. The voltage is combined is combined and provided to

the power amplifier unit. This is clearly shown in Figure 3 where the output of all of the voltage regulating units are coupled before being supplied to the respective power amplifier unit.

The voltage linear combination circuit contained in a single voltage regulator circuit of each inverter contributes only a portion of output to the parallel inverter system. If one inverter fails, its failure has minimal effect. Thus, the failure of one inverter does not significantly degrade the entire system.

Clearly, Kawabata does not include a plurality of inverters each having a voltage regulator with a voltage linear combination circuit. No linear combination circuit is taught or disclosed in Kawabata, and no such circuit is needed in Kawabata because Kawabata only addresses voltage regulation in a single inverter, not across multiple parallel inverters. In Kawabata, no voltages are linearly combined across a configuration of parallel devices. Although in Kawabata, voltages may be regulated and combined at node 124, such operation is done within the confines of a single inverter circuit, and such operation does not span multiple inverter circuits. In summary, Kawabata does not teach or suggest a voltage linear combination circuit in each voltage regulator that linearly combines all of the output voltages of each of the voltage regulators in each of the inverter circuits.

Because at least one element of applicant's claimed invention is missing from the device in Kawabata, Kawabata cannot anticipate applicant's claimed invention. Accordingly, applicant asserts that independent claim 1 is allowable over Kawabata, and that dependent claims 2-9 are allowable as depending from an allowable base claim.

Rejection Under 35 U.S.C. §103

Claims 2 and 3 stand rejected under 35 U.S.C. §103 as being unpatentable over Kawabata in view of Deng (US 6,178,103), while claim 5 stands rejected under 35 U.S.C. §103 as being

unpatentable over Kawabata in view of Rehm (US 5,956,244). In view of the claims as presently amended, applicant respectfully traverses this rejection.

Regarding the rejection of claim 2, applicant reasserts the above arguments made in traversing the rejection based on §102 as support for traversing the rejection based on §103. Neither the primary reference to Kawabata nor the secondary reference to Deng, taken alone or in combination, teach or suggest applicant's claimed invention. The primary reference to Kawabata does not teach or suggest a voltage linear combination circuit in each voltage regulator that linearly combines all of the output voltages of each of the voltage regulators in each of the inverter circuits. Kawabata is completely deficient with respect to this element. Combining Kawabata with the secondary reference to Deng does not provide applicant's claimed invention because like, Kawabata, Deng is also deficient. Because Deng cannot add any elements missing from Kawabata, the combination of the primary and secondary references does not provide applicant's claimed invention.

Further, neither Kawabata nor Deng teaches an OC gate and fault shield switch (K2), as required by claim 2. In applicant's claimed invention, a square wave at the power frequency is output through an OC gate and a fault shield (K2). The OC gate and fault shield (K2) improve the reliability of the parallel inverter system because when a fault occurs at the front-end of fault shield (K2), the fault shield (K2) is opened, and the synchronizing square wave generator does not contribute to the output, thus shielding the system from the fault (specification, page 6, lines 32-34). Accordingly, applicant respectfully submits that neither Kawabata nor Deng, taken individually or in combination renders applicant's claimed invention obvious.

Regarding the rejection of claim 3, applicant reasserts the above arguments made in traversing the rejection based on §102 and traversing the rejection of claim 2 under §103. Again,

neither the Kawabata nor Deng, taken alone or in combination, teach or suggest a voltage linear combination circuit in each voltage regulator that linearly combines all of the output voltages of each of the voltage regulators in each of the inverter circuits. Kawabata is completely deficient with respect to this element. Further, neither Kawabata nor Deng teaches a fault shield switch (K3). The fault shield (K3) improves the reliability of the parallel inverter system. When a fault occurs at the front-end of (K3), K3 is opened, and the voltage given generator does not contribute to the output so as to protect the circuit (specification, page 7, lines 29-30). Accordingly, applicant respectfully submits that neither Kawabata nor Deng, taken individually or in combination, renders applicant's claimed invention obvious.

Regarding the rejection of claim 5 based on Kawabata and the secondary reference to Rehm, applicant reasserts the above arguments made in traversing the rejection based on §102 and traversing the rejection of claims 2-3 under §103. Again, neither the Kawabata nor Rehm, taken alone or in combination, teach or suggest a voltage linear combination circuit in each voltage regulator that linearly combines all of the output voltages of each of the voltage regulators in each of the inverter circuits. Rehm does not add any element that is already missing in Kawabata. Further, neither Kawabata nor Rehm teaches a voltage linear combination circuit having an output impedance and a fault shield switch (K4). The fault shield switch (K4) improves the reliability of the parallel inverter system. When a fault occurs at the front-end of the switch K4, the switch is opened to shield the system. Because the output of each voltage regulator circuit is linearly combined through the output impedance, the system functions normally when the switch K4 is opened (specification, page 8, lines 14-17). Accordingly, applicant respectfully submits that neither Kawabata nor Rehm, taken individually or in combination renders applicant's claimed invention obvious.

Summary

Pending claims 1-9 are patentable. Applicant respectfully requests the Examiner grant early allowance of this application. The Examiner is invited to contact the undersigned attorneys for the Applicant via telephone if such communication would expedite this application.

Respectfully submitted,

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